REMARKS

The application has been reviewed in light of the Office Action dated January 30, 2007. Claims 1-40 are pending in this application, with claims 1, 9, 17, 25, 29, 33 and 37-39 being in independent form.

Claims 1, 9, 17, 25, 29, 33 and 37-40 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Yoichiro et al. (JP06-317616) in view of U.S. Patent 5,481,469 to Brasen et al. Claims 2-8, 10-16, 18-23, 26-28, 30-32 and 34-36 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Yoichiro in view of Brasen and in further view of Microsoft Press Computer Dictionary, 1997 edition.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1, 9, 17, 25, 29, 33 and 37-39 are patentable over the cited art, for at least the following reasons.

This application relates to estimation of electric power consumption by integrated circuits comprised of basic cells and mega cells.

Applicant devised an improved approach which includes simulating logic of basic and mega cells of the integrated circuit, and estimating electric power consumed by mega cells of the integrated circuit based on the logic simulations and pre-established power consumption data. Estimation of electric power consumed by the mega cells includes estimating a current consumed by the mega cells by simulating logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells. Each of independent claims 1, 9, 17, 25, 29, 33 and 37-39 addresses these features, as well as additional features.

Yoichiro, as understood by Applicant, proposes a method for estimating power consumption of a digital circuit by performing simulation of the circuit. More specifically, Yoichiro proposes setting each element of the circuit with a DC power consumption value and initializing an AC power consumption value at commencement of simulation, simulating logic and as a logic state of an element changes adding an increment to the AC power consumption value.

As acknowledged in the Office Action, Yoichiro does not teach or suggest simulating and calculating the power consumed by a mega cell in the integrated circuit.

Moreover, Yoichiro does not several other features of the claimed subject matter of the present application.

For example, Applicant does not find teaching or suggestion in Yoichiro of (i) estimating a current consumed by the mega cells by simulating logic states for each mega cell, (ii) determining an average operation frequency for each logic state, and (iii) estimating a current consumed by the basic cells, as provided by the subject matter of claim 1 of this application.

The abstract of Yoichiro, which states as follows, clearly does not teach or suggest such features:

> PURPOSE: To carry out high speed measurement by providing the first memory means to store the value of electric power consumed in a state defined for each element, and the second memory means to store the total value of electric power consumed in simulation time.
> CONSTITUTION: *When simulation is started, a DC power consumption value register 204 is initialized on the total value of electric power in a DC power consumption value area 203 to all the elements in a circuit.* When the processing of simulation time is started, *an AC power consumption value register 202 is initialized.* Next, at the present simulation time, *the state of the element in the circuit is judged on the state of a nodal point in the circuit* and the inner state of the element, and the processing is repeated to the element altered in its state. In the case of renewing the register 202, *the power consumption value corresponding to the state of the element is read out of an AC power consumption value register 201, and added to the register*

> *202*. In the case of renewing the DC power consumption value, *the read out value is subtracted from a register 204 corresponding to the state before alteration*, and all the elements altered in their states are processed in this way.

Yoichiro (abstract as well as other portions), contrary to the contention in the Office Action, simply does not teach or suggest (i) estimating a current consumed by the mega cells by simulating logic states for each mega cell, (ii) determining an average operation frequency for each logic state, and (iii) estimating a current consumed by the basic cells, as provided by the subject matter of claim 1 of this application.

Brasen, as understood by Applicant, proposes an approach for automatic power vector generation for sequential circuits including performing logic simulation only for basic cells (i.e. logic gates and the like). A block BLOCK2 (see FIGS. 7 and 8) of Brasen is the sole disclosure in Brasen of a mega-cell.

It is contended in the Office Action that Brasen proposes simulation and calculation of power consumed by a mega-cell in an integrated circuit.

However, Brasen states that the mega-cell is a RAM or ROM which has "fixed power requirements". Since Brasen states that the mega-cell described therein has fixed power requirements, one skilled in the art would not understand Brasen to be teaching or suggesting that logic simulation is needed for estimation of power consumption by the mega-cell.

Further, Brasen, like Yoichiro, fails to teach or suggest estimation of electric power consumption by integrated circuits which includes, amongst other acts, (i) estimating a current consumed by the mega cells by simulating logic states for each mega cell, (ii) determining an average operation frequency for each logic state, and (iii) estimating a current consumed by the basic cells, as

provided by the subject matter of claim 1 of this application.

The Office Action cites the Microsoft Press Computer Dictionary as purportedly proposing use of various computer readable media for storing executable code.

Applicant does not find teaching or suggestion in the cited art, however, of a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit, which comprises (a) estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells, (b) estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the basic cells, and (c) combining the first and second values to obtain the power consumption of the integrated circuit, as provided by the subject matter of independent claim 1 of the present application.

Independent claims 9, 17, 25, 29, 33 and 37-39 are patentably distinct from the cited art for at least similar reasons.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1, 9, 17, 25, 29, 33 and 37-39, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in

condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any fees that may be required in connection with this Response and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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